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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/811,811	03/30/2004	Yasuhiro Takeda	57810-095	2835

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EXAMINER	
LANDAU, MATTHEW C	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 08/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/811,811	TAKEDA ET AL.	
	Examiner	Art Unit	
	Matthew Landau	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) *18-30* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17 and 31-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of Group I (claims 1-17), in the reply filed on December 29, 2005 is acknowledged.

Upon further review, the Examiner has discovered the previous election of species requirement was improper since the species are disclosed as usable together. Therefore, those claims previously withdrawn as being drawn to a non-elected species will now be examiner. However, the claims drawn to Group II (claim 18-30) remain withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Ono et al. (US Pat. 6,436,783, hereinafter Ono).

Regarding claims 1, 3, 4, and 5, Figures 1-4 and 7-9 of Ono disclose a semiconductor device comprising: a first conductivity type semiconductor region (silicon substrate 1) (col. 11, lines 63-65) having a main surface (upper surface); an element isolation region 2 isolating an

active region; a second conductivity type source/drain region (16/22) formed on said main surface to hold a channel region therebetween at a prescribed interval; a gate electrode 20 formed on said channel region through a gate insulator film 7; and side wall insulator films 18 (silicon oxide) (col. 21, lines 53-55) formed on the side surfaces of said gate electrode. Ono discloses fluorine has been introduced into the channel region (col. 13, lines 10-12). The channel region extends over a junction interface between the source/drain regions (16/22) and the substrate 1. Therefore, Figures 1-4 of Ono disclose fluorine has been introduced a region extending over from the element isolation region over a junction interface between said first conductivity type region and said second conductivity type source/drain regions. It is considered that "a region" is a region extending from the isolation region including the source/drain region and the channel. Since the fluorine is at least in the channel, the fluorine is in the claimed region. Note that the claim does not require fluorine to be in every part of the region.

Regarding claims 2 and 8, Ono also discloses fluorine is introduced into the interface between the gate insulator film and the central region of said channel region (col. 21, lines 38-41) as well as said gate insulator film 7. Note that Ono discloses the amount of fluorine introduced into the gate insulator is reduced and that "almost" no fluorine is in the gate insulator film (col. 8, lines 16-18 and 48-50). Therefore, there is at least some fluorine in the gate insulator film.

Regarding claim 7, Ono also discloses the sidewalls can be formed prior to the fluorine implantation (col. 16, lines 49-51). Therefore, it would be inherent that at least some fluorine is introduced into the side wall insulator films during the implantation step.

Regarding claim 9, Figures 7-9 of Ono disclose a semiconductor device comprising: a first conductivity type semiconductor region (silicon substrate 1) (col. 11, lines 63-65) having a main surface (upper surface); a second conductivity type source/drain region (16/22) formed on said main surface to hold a channel region therebetween at a prescribed interval; a gate electrode 20 formed on said channel region through a gate insulator film 7; and side wall insulator films 18 (silicon oxide) (col. 21, lines 53-55) formed on the side surfaces of said gate electrode. Ono discloses performing a fluorine implantation after forming the side wall insulators 18 (col. 16, line 49-51). Therefore, it is inherent that at least some fluorine is introduced into the side wall insulator films during the implantation step. Fluorine inherently reduces the dielectric constant.

Regarding claim 12, Figures 7-9 of Ono disclose fluorine is introduced also into regions extending over the junction interfaces between said first conductivity type semiconductor region and said second conductivity type source/drain regions. Ono discloses fluorine has been introduced into the channel region (col. 13, lines 10-12). The channel region extends over a junction interface between the source/drain regions (16/22) and the substrate 1.

Regarding claims 13-15, Figures 7-9 of Ono disclose a semiconductor device comprising: a first conductivity type semiconductor region (silicon substrate 1) (col. 11, lines 63-65) having a main surface (upper surface); a second conductivity type source/drain region (16/22) formed on said main surface to hold a channel region therebetween at a prescribed interval; a gate electrode 20 formed on said channel region through a gate insulator film 7, wherein a halogenic element (fluorine) is introduced into the interface between the gate insulator film and the central region of said channel region (col. 21, lines 38-41) as well as said gate insulator film 7. Note that Ono discloses the amount of fluorine introduced into the gate insulator is reduced and that "almost"

no fluorine is in the gate insulator film (col. 8, lines 16-18 and 48-50). Therefore, there is at least some fluorine in the gate insulator film.

Regarding claim 16, Ono discloses performing a fluorine implantation after forming the side wall insulators 18 (col. 16, line 49-51). Therefore, it is inherent that at least some fluorine is introduced into the side wall insulator films during the implantation step.

Regarding claim 17, Figures 7-9 of Ono disclose fluorine is introduced also into regions extending over the junction interfaces between said first conductivity type semiconductor region and said second conductivity type source/drain regions. Ono discloses fluorine has been introduced into the channel region (col. 13, lines 10-12). The channel region extends over a junction interface between the source/drain regions (16/22) and the substrate 1.

Regarding claims 31-33, Figures 7-9 of Ono disclose a semiconductor device comprising: a first conductivity type semiconductor region (silicon substrate 1) (col. 11, lines 63-65) having a main surface (upper surface); a second conductivity type source/drain region (16/22) formed on said main surface to hold a channel region therebetween at a prescribed interval; a gate electrode 20 formed on said channel region through a gate insulator film 7; and side wall insulator films 18 (silicon oxide) (col. 21, lines 53-55) formed on the side surfaces of said gate electrode. Ono discloses performing a fluorine implantation after forming the side wall insulators 18 (col. 16, line 49-51). Therefore, it is inherent that at least some fluorine is introduced into the side wall insulator films during the implantation step. Ono also discloses fluorine is introduced also into regions extending over the junction interfaces between said first conductivity type semiconductor region and said second conductivity type source/drain regions. Ono discloses fluorine has been introduced into the channel region (col. 13, lines 10-12). The channel region extends over a

junction interface between the source/drain regions (16/22) and the substrate 1. Ono also discloses fluorine is introduced into the interface between the gate insulator film and the central region of said channel region (col. 21, lines 38-41) as well as said gate insulator film 7. Note that Ono discloses the amount of fluorine introduced into the gate insulator is reduced and that "almost" no fluorine is in the gate insulator film (col. 8, lines 16-18 and 48-50). Therefore, there is at least some fluorine in the gate insulator film. Further regarding claim 32, Figure 4 of Ono discloses a wire 29 is connected to the surface of said second conductivity type impurity regions corresponding to said region introduced with said element through a contact hole.

Regarding claim 34, it is considered that "a region" is a region extending from the isolation region including the source/drain region and the channel. Since the fluorine is at least in the channel, the fluorine is in the claimed region. Note that the claim does not require fluorine to be in every part of the region.

Claims 5 and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Mandelman et al. (US PGPub 2003/0020125, hereinafter Mandelman).

Regarding claim 5, Figure 10 of Mandelman discloses a semiconductor device comprising: a first conductivity type semiconductor region (substrate 10) having a main surface; an element isolation region 20 isolating an active region; and a second conductivity type impurity region (90/95/130) formed on said main surface of said semiconductor region, wherein an element of carbon has been introduced into a region (97/99) extending from the isolation region over a junction interface between said first conductivity type semiconductor region and

said second conductivity type impurity region (paragraph [0050]). It is considered that "a region" is a region extending from the isolation region including the source/drain region and the area beneath the gate. Since the carbon is in the area beneath the gate, carbon has been introduced into the claimed region. Note that the claim does not require carbon to be in every part of the region.

Regarding claim 6, Figure 10 of Mandelman discloses said impurity region (90/95/130) includes a low-concentration impurity region (90/95) (LDD regions) (paragraph [0050]) and a high concentration impurity region 130 (source/drain region), and said element of carbon is introduced into at least a region (97/99) extending over the junction interface between said first conductivity type semiconductor region and said high-concentration impurity region. Note that Figure 10 shows regions 97 and 99 extend over a part of the junction interface between the source/drain regions 130 and the substrate.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 32-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mandelman in view of Ono.

Regarding claims 32 and 35, Figure 10 of Mandelman discloses a semiconductor device comprising: a first conductivity type semiconductor region (substrate 10) having a main surface;

an element isolation region 20 isolating an active region; and a second conductivity type impurity region (90/95/130) formed on said main surface of said semiconductor region, wherein an element of carbon has been introduced into a region (97/99) extending from the isolation region over a junction interface between said first conductivity type semiconductor region and said second conductivity type impurity region (paragraph [0050]). Figure 10 of Mandelman further discloses said impurity region (90/95/130) includes a low-concentration impurity region (90/95) (LDD regions) (paragraph [0050]) and a high concentration impurity region 130 (source/drain region). The difference between Mandelman and the claimed invention is a wire connected to the surface of said second conductivity type impurity regions corresponding to said region introduced with said element through a contact hole. Figure 4 of Ono discloses a wire 29 is connected to the surface of said second conductivity type impurity regions (source/drain regions) 22 through a contact hole. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Mandelman by including a wire connected to the source/drain regions 130 through a contact hole for the purpose of making electrical connection to said regions.

Regarding claim 33, Figure 10 of Mandelman discloses side wall insulator films 140 on the side surfaces of said gate electrode 80.

Regarding claim 34, it is considered that "a region" is a region extending from the isolation region including the source/drain region and the area beneath the gate. Since the carbon is in the area beneath the gate, carbon has been introduced into the claimed region. Note that the claim does not require carbon to be in every part of the region.

Response to Arguments

Applicant's arguments filed May 23, 2006 have been fully considered but they are not persuasive.

Applicant argues that Ono does not disclose a region containing fluorine or carbon extending from an element isolation region as claimed. As explained in the above rejection, "a region" can be considered an arbitrary region extending from the isolation region. It has been considered that "a region" is a region extending from the isolation region including the source/drain region and the channel. Since the fluorine is at least in the channel, the fluorine is in the claimed region. Note that the claim does not require fluorine to be in every part of the region. Note that Applicant makes similar arguments regarding Mandelman.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Landau whose telephone number is (571) 272-1731.

The examiner can normally be reached from 8:30 AM - 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for regular communications and (571) 273-8300 for After Final communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should any questions arise regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Matthew C. Landau

August 5, 2006